REMARKS

The Office Action of September 14, 2005 has been received and reviewed. The Examiner is thanked for reviewing this application.

Claims 1-20 and 22-24 were pending prior to the instant amendment, claim 21 was cancelled, and claims 2-3, 10-16 and 23-24 were withdrawn from consideration. By this amendment, claim 1 has been amended, and claims 2-3 and 10-16 have been canceled, and new claims 25-61 have been added. Accordingly, claims 1, 4-9, 17-20, 22 and 25-61 are pending for consideration, of which claims 1, 26-27, 44-46 are independent.

Referring now to the detailed Office Action, claims 1, 4-6, 9, 17-20 and 22 stand rejected under 35 U.S.C. §103(a) as being obvious over Kawasaki et al. (U.S. Patent No. 6,424,012 – hereafter Kawasaki) in view of Ogawa et al. (U.S. Patent No. 6,362,507 – hereafter Ogawa). Further, claim 7 stands rejected under 35 U.S.C. §103(a) as being obvious over Kawasaki in view of Ogawa and Someya et al. (U.S. Patent Publication No. 2002/0080295 – hereafter Someya). Still further, claim 8 stands rejected under 35 U.S.C. §103(a) as being obvious over Kawasaki in view of Ogawa and Murade (U.S. Patent Publication No. 2001/0030722 – hereafter Murade). These rejections are respectfully traversed at least for the reasons provided below.

In the rejection of claim 1, the Examiner asserted that Kawasaki discloses a semiconductor device having:

a) the pixel TFT has a channel formation region (407) formed over a first wiring line (403) with an insulating layer (402) interposed, and has a low concentration impurity region (406) that is in contact with the channel formation region and overlaps the first wiring line (for example: see Fig. 8b);

b) the storage capacitor is formed: from a capacitor wiring line (415), a semiconductor region (414) that has the same composition as the channel formation region or the low concentration impurity region, and a part of the insulating layer and wherein the first wiring line and the capacitor wiring line are formed on the same layer (for example: see Fig. 8b); and

c) wherein a second wiring line (416) is formed over the channel formation region with a second insulating layer (419) interposed therebetween (for

example: see Fig. 8b).

The Examiner further asserted that Ogawa discloses the use of a second wiring line (846) that does not overlap the low concentration impurity region, as shown in Fig. 19 of Ogawa.

In response to the rejection of claim 1, Applicants have amended claim 1, as shown above, to improve the claim language and to further distinguish the claimed invention over Kawasaki and Ogawa. Specifically, claim 1 has been amended to delete the recitation "wherein a second wiring line is formed over the channel formation region with a second insulating layer interposed therebetween; and wherein a second wiring line does not overlap the low concentration impurity region" and to include the recitation "a gate electrode is formed over the channel formation region with a second insulating layer interposed therebetween; wherein the gate electrode does not overlap the low concentration impurity region". Support for the amendment can be found at least in, e.g, Fig. 2A and its associated description in the specification.

Applicants respectfully assert that Kawasaki and Ogawa fail to teach, disclose or suggest the amended claimed feature wherein a gate electrode is formed over the channel formation region with a second insulating layer interposed therebetween, and wherein the gate electrode does not overlap the low concentration impurity region, as recited in the amended claim 1.

The amendment of claim 1 and the arguments relating to the rejection of claim 1 are also applicable to the rejection of claims 4-9, 17-20 and 22. Hence, in the interest of keeping prosecution history compact, Applicants will not traverse each and every rejection of the dependent claims. Applicants reserve the right to do so in the future, as necessary.

Further, with regard to claim 9, Applicants respectfully assert that neither Kawasaki nor Ogawa teaches, discloses, or suggests the claimed feature wherein the storage capacitor is formed under the source wiring line and/or the gate wiring line.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference

(or references when combined) must teach or suggest all of the claim limitations. As Kawasaki and Ogawa are deficient as discussed above, their combination in the pending §103(a) rejections are improper.

New claims 25-61 have been added to further complete the scope to which Applicants are entitled. Claims 25-61 includes all the features of amended claim 1 and, hence, should also be allowable.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1, 4-9, 17-20, 22 and 25-61 be allowed, and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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